Sri Sathya Sai College for Women, Bhopal

(An Autonomous College affiliated to Barkatullah University, Bhopal)

(NAAC Accredited 'A' Grade)

SYLLABUS

SESSION: 2023-24

PROGRAM: Certificate

YEAR: I Year

CLASS: B.Sc.

SUBJECT: Computer Science

Sri Sathya Sai College for Women, Bhopal
(An Autonomous College Affiliated to Barkatullah University Bhopal)
Department of Higher Education, Govt. of M.P.
Under Graduate Syllabus (Annual Pattern)
As recommended by Central Board of Studies and approved by the Governor of M. P.
wef 2021-2022
(Session 2023-24)
(NEP-2020)

Class	**B.Sc.**
Year	**I Year**
Subject	**Computer Science**
Course Title	**Computer System Architecture**
Course Type	**Core Course (Major I)**
Credit Value	**4**
Max. Mark	**30+70 (Minimum Marks 35)**

Course Outcome: After the completion of this course, a student shall be able to:

- Understand the basic structure, operation and characteristics of digital computer.
- Be able to design simple combinational digital circuits based on given parameters.
- Familiarity with working of arithmetic and logic unit as well as the concept of pipelining.
- Know about hierarchical memory system including cache memories and virtual memory.
- Understand concept and advantages of parallelism, threading, multiprocessors and multicore processors.
- Know the contributions of Indians in the field of computer architecture and related technologies.

Particular

Unit I	**Fundamentals of Digital Electronics**: Data Types, Complements, Fixed-Point Representation, Floating-Point Representation, Binary and other Codes, Error Detection Codes. **Logic Gates**, Boolean Algebra, Map Simplification, Combinational Circuits, Sequential Circuits, simple combinational circuit design problems. **Circuits**- Adder- Subtractor, Multiplexer, Demultiplexer, Decoders, Encoders, Flip - Flops, Registers, Counters.
Unit II	**Basic Computer Organization**: Instruction codes, Computer Registers, Computer Instructions, Timing & Control, Instruction Cycles, Memory Reference Instruction, Input - Output & Interrupts, Complete Computer Description & Design of Basic Computer.
Unit III	**Instructions** - Instruction formats, Addressing modes, Instruction codes, Machine language, Assembly language. **Register Transfer and Micro operations** - Register Transfer Language, Register Transfer, Bus & Memory Transfer, Arithmetic Micro-operations, Logic Micro-operations, Shift Micro-operations.
Unit IV	**Processor and Control Unit** - Hardwired vs. Micro programmed Control Unit, General Register Organization, Stack Organization, Instruction Format, Data Transfer & Manipulation, Program Control, Introductory concept of RISC, CISC, advantages and disadvantages of both.

	Pipelining – concept of pipelining, introduction to Pipelined data path and control – Handling Data hazards & Control hazards.
Unit V	**Memory and I/O Systems** - Peripheral Devices, I/O Interface. **Data Transfer Schemes** - Program Control, Interrupt, DMA Transfer, I/O Processor. **Memory Hierarchy**, Processor vs. Memory Speed, High-Speed Memories, Main memory, Auxiliary memory, Cache Memory, Associative Memory, Interleaving, Virtual Memory, Memory Management.
Unit VI	**Parallelism** – meaning, types of parallelism, introduction to Instruction-level-parallelism, Parallel processing challenges, Applications. **Flynn's classification** – Introduction to SISD, SIMD, MISD, MIMD **Hardware multithreading** – Introduction, types, advantages and applications. **Multicore processors** – Introduction, advantages, difference from multiprocessor.
Unit VII	**Indian contribution to the field** – Contributions of reputed scientists of Indian origin - like - Dr. Vinod Dham – Father of Intel Pentium Processor, Dr. Ajay Bhat – Co-Inventor of USB Technology, Dr. Vinod Khosla- co-founder of Sun Microsystems, Dr. Vijay P Bhatkar - architect of India's national initiative in supercomputing, and many others. **Parallel Computing projects of India** – PARAM, ANUPAM, FLOSOLVER, CHIPPS etc. Other relevant contributors and contributions.
Keywords/Tags:	Digital Electronics, Logic Gates, Circuits, Instruction formats, Addressing Modes, Parallelism, Pipelining, Memory Hierarchy, Multicore, Multithreading, SISD, SIMD, MISD, MIMD, PARAM, ANUPAM, FLOSOLVER, CHIPPS

Suggestion Books:

- M. Morris Mano, "Computer System Architecture", PHI.
- Heuring Jordan , "Computer System Design & Architecture" (A.W.L.)
- William Stalling, "Computer Organization & Architecture", Pearson Education Asia.
- V. Carl Hamacher, "Computer Organization", TMH
- Tannenbaum, "Structured Computer Organization", PHI.

Suggestive digital platform web links

https://www.youtube.com/watch?v=4TzMyXmzL8M
https://nptel.ac.in/courses/106/106/106106166/
https://nptel.ac.in/courses/106/106/106106134/

Suggested equivalent online courses

https://nptel.ac.in/courses/106/105/106105163/

Scheme of Marks:

Maximum Marks: 100		
Continuous Comprehensive Evaluation (CCE): 30 marks, Term End Exam Theory: 70 marks		
Internal Assessment: Continuous Comprehensive Evaluation (CCE):	Class Test Assignment/ Presentation	**30**
External Assessment: University Exam Section Time:03.00 Hours	**Section (A)** Very Short questions **Section (B)** Short questions **Section (C)** Long questions	**70**
		Total 100

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Class	**B.Sc.**
Year	**I Year**
Subject	**Computer Science**
Course Title	**Computer Architecture Lab**
Course Type	**Core Course (Major I)**
Credit Value	**2**
Max. Mark	**30+70 (Minimum Marks 35)**

Course Outcome: After the completion of this course, a student shall be able to do the following:

- Realization of the basic logic and universal gates.
- Verify the behavior of logic gates using truth tables.
- Implement Binary-to -Gray, Gray-to -Binary code conversions
- Design half and full adder circuit using basic gates.
- Design and construct flip flops and verify the excitation tables.

Particular

List of Practicals:

1. To study basic gates (AND, OR, NOT) and verify their truth tables.
2. To convert a given binary number to Gray code using IC 7486.
3. To study and verify NAND as Universal gate using IC 7400.
4. To study Half Adder using basic gates and verify its truth table.
5. To study Full Adder using basic gates and verify its truth table.
6. To realize basic gates (AND, OR, NOT) from Universal gates (NAND and NOR).
7. To verify truth table of 4-bit adder using IC 7483.
8. To design and construct RS flip Flop using gates and verify the truth table.
9. To design and construct JK flip Flop using gates and verify the truth table.
10. To verify DeMorgan's Theorem.

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Suggested equivalent online courses:

https://nptel.ac.in/courses/106/105/106105163/

Scheme of Marks:

Maximum Marks: 100		
Internal Assessment :	Class Interaction / Quiz Attendance Assignments (Charts / Model Seminar / Rural Service / Technology Dissemination / Report of Excursion / Lab Visits / Survey / Industrial visit)	**30**
External Assessment:	Viva Voce on Practical Practical Record File Table Work / Experiments	**70**
		Total 100